

REMARKS/ARGUMENTS

Reconsideration of the application as amended is respectfully requested.

Status of Claims

Claims 1-26 are pending in the application, with claim 1 being the only independent claim. Claims 1 and 8 have been amended. No new matter has been added.

Overview of the Office Action

Claims 1-4, 6, 7, 12, 13, 22 and 23 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,583,443 (*Chang*).

Claims 5, 8, 9 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of U.S. Patent No. 5,717,226 (*Lee*).

Claims 10, 11, 25 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of U.S. Patent No. 6,346,719 (*Udagawa*).

Claims 14-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of JP 2001036131 (*Udagawa II*).

Summary of Subject Matter Disclosed in the Specification

The following descriptive details are based on the specification. They are provided only for the convenience of the Examiner as part of the discussion presented herein, and are not intended to argue limitations which are unclaimed.

The specification of the present application discloses a light-emitting diode chip having an epitaxial semiconductor layer sequence with an active zone that emits electromagnetic radiation, and an electrical contact structure. The electrical contact structure comprises a radiation-transmissive electrical current expansion layer which contains ZnO, and an electrical connection layer. The current expansion layer is applied directly on a cladding layer of the semiconductor layer sequence on which the connection layer is also applied directly (*see* paragraphs [0007], [0035] and [0037] of the original specification). The cladding layer is p-doped (*see* paragraphs [0015] and [0034] of the original specification).

The connection layer is electrically conductively connected to the current expansion layer and has a junction with the cladding layer. When an electrical voltage is applied to the light-emitting diode chip in the operating direction, the junction between the connection layer and the cladding layer is not electrically conductive or is only poorly electrically conductive so that the entire, or virtually the entire, current flows via the current expansion layer into the semiconductor layer sequence (*see* paragraph [0007] of the original specification), rather than directly from the connection layer to the cladding layer to which the connection layer is directly applied.

During operation, as a result of this structure, no current, or at least less current, is injected into the region directly below the connection layer. Therefore, no light, or at least less light, is generated in this region and absorbed by the connection layer (*see* paragraph [0008] of the original specification).

Arguments

Independent Claim 1

Independent claim 1 has been amended to include a feature of claim 9. Claim 1 now recites:

“wherein the current expansion layer is applied directly on a cladding layer of the semiconductor layer sequence and comprises a window, in which the connection layer is applied directly on said cladding layer of the semiconductor layer sequence, and said cladding layer is p-doped;

wherein a junction between the connection layer and the cladding layer, during operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer flows via the current expansion layer into the semiconductor layer sequence” (emphasis added).

Claim 1 is not anticipated by *Chang* because *Chang* does not disclose, either expressly or inherently, each and every element set forth in amended claim 1. In particular, *Chang* does not disclose, teach or suggest the above-highlighted limitations of claim 1.

Chang relates to a light-emitting diode comprising an epi-LED stack structure, where a transparent conductive layer 44 and a metal layer 48B are disposed on the epi-LED stack structure. See Fig. 4C; Abstract; and col. 3, lines 46-55 of *Chang*.

The Examiner refers to Fig. 4C of *Chang*, and contends that claim 1 reads on *Chang*. However, according to *Chang*, the transparent conductive layer 44 and the metal layer 48B form an n-type ohmic contact (see col. 5, lines 27-32 of *Chang*). The n-type ohmic contact is disposed on an etching stop layer 24 or an n-doped cladding layer 22 on the n-type side of the epi-LED

stack structure (*see* col. 3, lines 56-59 of *Chang*). In other words, in *Chang*, both the transparent conductive layer 44 and the metal layer 48B are on the n-doped cladding layer 22. Thus, *Chang* does not disclose, teach or suggest that a current expansion layer or a connection layer is applied directly on a p-doped cladding layer.

In sharp contrast, amended claim 1 of the present application recites “wherein the current expansion layer is applied directly on a cladding layer of the semiconductor layer sequence and comprises a window, in which the connection layer is applied directly on said cladding layer of the semiconductor layer sequence, and said cladding layer is p-doped” (emphasis added).

The Examiner implicitly acknowledges these differences between *Chang* and amended claim 1 because the Examiner rejects claim 9 (a feature of which is now included in claim 1) under 35 U.S.C. §103(a), not under 35 U.S.C. §102(e).

In addition, *Chang* does not disclose any current barrier between the metal layer 48B and the etching stop layer 24 or the n-doped cladding layer 22 (when the metal layer 48B is disposed directly on the n-doped cladding layer 22). In *Chang*, the metal layer 48B is directly applied in the usual way on the etching stop layer 24 or the n-doped cladding layer 22 (*see* Fig. 4C; and col. 6, lines 1-11 of *Chang*). Thus, the metal layer 48B has a direct and good electrical contact with the etching stop layer 24 or the n-doped cladding layer 22. As a result, during operation, a significant current flows from the metal layer 48B directly into the etching stop layer 24 or the n-doped cladding layer 22.

Chang mentions that the metal layer 48B has an altitude which is higher than the surface level of the transparent conductive layer 44, and that the contact between the metal layer 48B and the transparent conductive layer 44 is of Shockley contact (*see* col. 6, lines 11-19 of *Chang*), but contrary to the Examiner’s interpretation, none of these features would render the contact

between the metal layer 48B and the etching stop layer 24 or the n-doped cladding layer 22 to be not electrically conductive or only poorly electrically conductive.

In sharp contrast, claim 1 recites “wherein a junction between the connection layer and the cladding layer, during operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer flows via the current expansion layer into the semiconductor layer sequence” (emphasis added).

In view of these differences, withdrawal of the §102(e) rejection of claim 1 is respectfully requested.

It is noted that *Chang* does not address the issue addressed by and the functionality provided by the claimed invention -- i.e., less current injection into the region directly below the connection layer; no light or at least less light generation in this region; and therefore no light or at least less light consumption by the connection layer. Thus, the above-discussed differences between claim 1 and *Chang* clearly and patentably distinguish claim 1 thereover under 35 U.S.C. §103(a).

The remaining cited references fail to bridge the above-discussed gap between claim 1 and *Chang*. Thus, claim 1 clearly and patentably distinguishes the present invention over the cited references when applied singly or in combination.

Dependent Claims 2-26

Claims 2-26 depend, either directly or indirectly, from independent claim 1 and, as such, each is respectfully deemed to be allowable therewith.

In addition, these claims include features which serve to even more clearly distinguish the claimed invention over the prior art of record.

Conclusion

Based on all of the above, it is respectfully submitted that the present application is now in full and proper condition for allowance. Prompt and favorable action to this effect, and early passage of the application to issue, are respectfully solicited.

Should the Examiner have any comments, questions, suggestions or objections, the Examiner is respectfully requested to telephone the undersigned in order to facilitate a resolution of any outstanding issues.

It is believed that no fees or charges are required at this time in connection with the present application. However, if any fees or charges are required at this time, they may be charged to our Patent and Trademark Office Deposit Account No. 03-2412.

Respectfully submitted,

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